ABSOLUTE BINARY PROGRAM NO. 24317-16001
DATE CODE 1431

SHIFT-ROTATE INSTRUCTIONS DIAGNOSTIC

reference manual

For HP 2100 Series and
HP 1000 Series Computers

NOTICE

The absolute binary code for this diagnostic is contained on one or more media (e.g., paper tape, cartridge tape, disc, and magnetic tape). The binaries also exist on single as well as multiple files. For the current date code(s) associated with these media, refer to appendix A in the *Diagnostic Configurator Reference Manual*, part no. 02100-90157, dated August 1976 or later.

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Introduction

This diagnostic program checks all code combinations of the Shift-Rotate Instruction Group for the 2100 Series and 1000 Series Computers. (For a summary of the instructions, see Appendix A. Further explanation is found in the *HP Assembler* manual, HP Product No. 02116-9014). The secondary objective is checking instructions and conditions affecting the overflow register. Included are special case tests of eight rotate instructions which involve the E-register.

This diagnostic should be preceded by the execution of the HP 2100, HP 1000 Series Alter-skip Instruction Diagnostic and the HP 2100, HP 1000 Series Memory Reference Instruction Diagnostic since instructions verified by those diagnostics are used to verify the Shift-Rotate instruction group.

Instruction test failures are communicated to the operator by means of register-coded HALTS through the computer memory data register (referred to as the MDR or T-register).

GENERAL ENVIRONMENT

Hardware Requirement

The diagnostic can be run on any 2100 Series or 1000 Series Computer. It does not require a system console device (e.g. teletype) or any other peripherals to run the test. A paper tape reader is required to load the diagnostic only.

Software Requirement

The required software consists of the Shift-Rotate Instructions Diagnostic binary object tape, part no. 24317-16001, and the Binary Loader (usually memory resident). See the appropriate *Front Panel Procedures* for the 2100 or 1000 Series Computer being used, for use of the Binary Loader. The Basic Binary Loader and the Basic Binary Disc Loader are described in the HP manual *Basic Binary Loader — Basic Binary Disc Loader* (HP Part No. 5951-1376).

This program does *not* use the Diagnostic Configurator. However, locations 100_8 to 127_8 are not used by this diagnostic and are available for use by the Diagnostic Configurator.

Operating Procedures

Operating procedures are divided into three parts: Preparation for Diagnostic Run, Running the Diagnostic, and Diagnostic Halts.

PREPARATION FOR DIAGNOSTIC RUN

The user loads the diagnostic using the Binary Loader. He may ensure that the proper diagnostic is loaded by verifying that the Diagnostic Serial Number in location 126_8 = 101002_8. No configuration procedures are required.

RUNNING THE DIAGNOSTIC

Except for the initial switch register entry, the diagnostic runs a complete cycle without operator intervention unless an error is found. Memory Data Register (T-register) HALTS indicate the type of error. When an error is detected, the operator may repeat the test sequence where the failure was detected.

Switch Options

Only switch register bits 12 and 0 have significance in this test. With both clear, the program will execute one pass and HALT with MDR=102077_8 unless an error is detected in Shift-Rotate instruction execution.

SWITCH 0. When set, this switch causes the program to repeat a failing Shift-Rotate instruction. A HALT is executed with MDR = 102076_8 just before repeating the instruction. Press RUN or SINGLE CYCLE to repeat instruction. (This switch does not apply to the Overflow Register tests.) See SHIFT-ROTATE TESTS in Error Analysis for further explanation.

SWITCH 12. When clear, this switch causes the program to execute a HALT with MDR=102077_8 at the end of each complete pass through the diagnostic. When set, the program cycles continuously, looping on the diagnostic.

a. Set program address register to 100_8.

b. Make desired switch register setting.

c. Press PRESET (EXTERNAL and INTERNAL, if applicable).

d. Press RUN.

Diagnostic Execution

Execution of the diagnostic proceeds automatically and requires 3 to 5 seconds to run.

DIAGNOSTIC HALTS

Three different error detection capabilities are provided: one for Shift-Rotate instruction tests, one for Overflow Register tests, and one for unexpected A- or B-register changes. Table 1 lists the error HALT codes and their significance.

Shift-Rotate Tests

Errors detected in these tests result in an MDR coded HALT of the general type $10200X_8$, where bits 0, 1, and 2 of X indicate the type (or types) of error detected:

- bit 0 = 1 indicates that the A- or B-register was found in error after the execution of a Shift-Rotate instruction that involved the register in error.
- bit 1 = 1 indicates an E-register error was detected.
- bit 2 = 1 indicates that an instruction involving a skip operation did not perform skip properly.

Along with the MDR coded HALT, additional error information is displayed in the following registers:

- A-register holds the actual A- or B-register result.
- B-register holds the expected A- or B-register result.
- E-register holds the actual E-register result.

Upon pressing the RUN switch, another HALT occurs with MDR = 102000_8. The following additional information is displayed:

- A-register holds the octal code of the failing Shift-Rotate instruction. Bit 11 of the displayed instruction identifies the register used: 0 indicates A-register, 1 indicates B.
- B-register holds the original data pattern contained in the A- or B-register.
- E-register holds the original contents of the E-register.

When RUN is pressed, following the second HALT executed, the program will continue if switch 0 is clear. If switch 0 is set, the original test values will be restored to registers and another HALT will occur with MDR = 102076_8. Upon pressing RUN again, the next instruction executed will be the failing instruction. The results can be closely studied by single stepping the program.

Overflow Tests

A failure detected by the Overflow register (OV) test results in a uniquely coded error HALT. See Table 1 for the summary of error HALTS.

Unexpected A- or B-register Changes

These errors are only detected in Shift-Rotate instructions. They are distinguished from those A- or B-register errors already discussed by the fact that these errors occur in the register that should *not* be affected by the tested Shift-Rotate instruction.

Before testing a Shift-Rotate instruction, the fixed non-symmetrical data pattern 173567_8 is placed in the register (A or B) not expected to change. If a change occurred in the register after executing the Shift-Rotate instruction, the following will happen:

- A HALT with MDR = 103000_8 for unexpected change to A-register.
- A HALT with MDR = 103001_8 for unexpected change to B-register.

The unexpected value will be left in the affected register and the other register will contain the octal code of the tested Shift-Rotate instruction. When RUN is pressed, the diagnostic will immediately continue unless switch 0 is invoked).

Table 1. Summary of Program Halts

Halt	Comments
10200*X*	Shift-Rotate Instruction error halt (See DIAGNOSTIC HALTS)
102000	Display halt following error halt (See DIAGNOSTIC HALTS)
102076	Halt before repeating failing Shift-Rotate instruction
102077	End of pass halt (A has # passes completed)
102040	CLO-SOC combination failed
102041	CLO-SOS combination failed
102042	STO-SOS combination failed
102043	STO-SOC combination failed
102044	STO-SOS,C combination failed
102045	SOS,C did not clear 0V
102050	A was 077777 and INA did not set 0V
102051	A was 177777 and INA set 0V
102052	Sum of 077777 and 077777 in A did not set 0V
102053	Sum of 100000 and 100000 in A did not set 0V
102054	Sum of 077777 and 100000 in A set 0V
102055	Sum of 177777 and 177777 in A set 0V
102056	Sum of 000000 and 000000 in A set 0V
102060	B was 077777 and INB did not set 0V
102061	B was 177777 and INB set 0V
102062	Sum of 077777 and 077777 in B did not set 0V
102063	Sum of 100000 and 100000 in B set 0V
102064	Sum of 077777 and 100000 in B set 0V
102065	Sum of 177777 and 177777 in B set 0V
102066	Sum of 000000 and 000000 in B set 0V
103000	Unexpected change in A-register (See DIAGNOSTIC HALTS)
103001	Unexpected change in B-register (See DIAGNOSTIC HALTS)
106077	Unexpected trap cell halt

Test Sections

The diagnostic is divided into two parts: Shift-Rotate instructions test and Overflow Register tests.

At the completion of each pass, the program will halt if switch 12 is clear. The halt code is 102077_8 and the pass count is displayed in the A-register. The A-register displays a 16 bit count.

SHIFT-ROTATE TESTS

All Shift-Rotate instructions are checked. Each valid instruction combination is checked 14 times. The 14 times consist of 7 different data patterns in either the A- or B-register depending on the instruction and for both values in the E-register.

Checked after the execution of each instruction are:

1. The contents of either the A- or B-register
2. The contents of the E-register
3. Whether or not the instruction skipped or didn't skip as expected

OVERFLOW TESTS

The overflow register tests follow the completion of all the Shift-Rotate instruction combinations. These tests are a string of individual tests and errors that result in a unique coded error halt which is read from the MDR. The halt codes and comments for the overflow register tests are summarized in Table 1.

No provisions are available for repeating failing overflow register tests.

APPENDIX A
Shift-Rotate Instructions Group

This group contains 19 basic instructions that can be combined to produce more than 500 different single cycle operations.

CLE	Clear E to zero
ALS	Shift A left one bit, zero goes to least significant bit. Sign unaltered
BLS	Shift B left one bit, zero goes to least significant bit. Sign unaltered
ARS	Shift A right one bit, extend sign; sign unaltered
BRS	Shift B right one bit, extend sign; sign unaltered
RAL	Rotate A left one bit
RBL	Rotate B left one bit
RAR	Rotate A right one bit
RBR	Rotate B right one bit
ALR	Shift A left one bit, clear sign, zero goes to least significant bit
BLR	Shift B left one bit, clear sign, zero goes to least significant bit
ERA	Rotate E and A right one bit
ERB	Rotate E and B right one bit
ELA	Rotate E and A left one bit
ELB	Rotate E and B left one bit
ALF	Rotate A left four bits
BLF	Rotate B left four bits
SLA	Skip next instruction if least significant bit in A is zero
SLB	Skip next instruction if least significant bit in B is zero